Mega ST Series

Internal

Expansion Bus Documentation

INTRODUCTION

The Atari Mega ST computer family has an expansion bus capable of supporting one internal expansion card. This document is intended to present, or provide references to, all of the necessary technical information to design a card which utilizes this bus.

Atari Corporation is not responsible for any misuse or misinterpretation of the information contained in this document. Nor do they guarantee its correctness or completeness. All information contained herein is subject to change without notice.

The supplier of an expansion card for the Atari Mega ST series of computer is responsible for insuring compliance with, and where necessary obtaining certifications for FCC, FTZ, UL and/or any other applicable approvals. It is also their responsibility to insure that the heat produced by the additional card is properly dissipated in all configurations of Mega ST series and that the card does not interfere with the normal operation of the ST.

Mechanical Description

Two sizes of expansion card are supported. One, the half card, is half the depth of the Mega ST unit (See figure 1). The other, the full card, is the full depth of the unit (See figure 2). In either case, the card butts up to the rear panel of the ST unit which has been provided with a removeable hatch through which connectors and/or cables can be mounted.

The expansion card connects to the ST motherboard through a 64 pin connector mounted on the bottom (solder) side of the expansion board. This connector plugs directly into its mate mounted on the motherboard. Standoffs, 25mm in length, are mounted into the bottom case through the motherboard. The expansion card is then screwed down to the standoffs. The standoffs and screws are not supplied with the mega ST and thus should be included with the expansion card. A hole located in the left rear of the expansion card fits around a plastic stud to provide extra strain relief for rear mounting connectors (See diagrams).

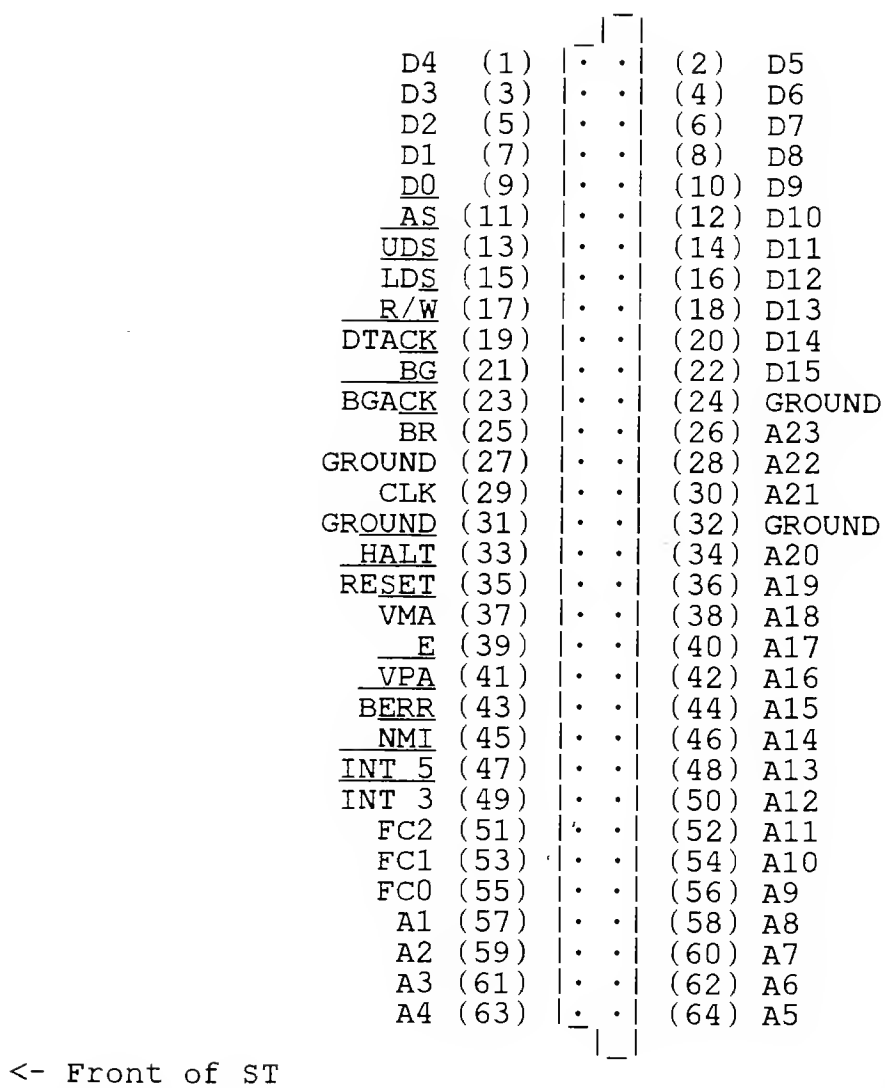
Electrical Description

The signals provided on the 64 pin connector are essentially the pins of the 68000 processor. These signals are all unbuffered. They are intended to drive one LS TTL load on the expansion board. Driving more than one load or driving excessive capacitance may cause improper ST operation. For this reason it is not acceptable to connect to the expansion connector in any manner other than the one outlined in the previous section (e.g. connecting directly with a cable is not acceptable).

The bus may be arbitrated away from the processor using the normal 68000 protocol. However, the bus grant signal provided on the connector is the end of the daisy chain. Response time will be effected by other DMA going on in the system (e.g. disk activity, hardware bit-blt transfers, etc.). If the peripheral requires DMA to occur while interrupts are enabled, care must be taken to limit the transfers to bursts of less than about 50 bus cycles allowing adequate time between bursts to process the interrupts.

The timing of the bus is that of an 8 MHz 68000 processor. Since the signals provided are essentially the processor pins, connecting peripherals in the same manner as you would to any 8 MHz 68000 should work with no problem. DMA is the exception. The bus cycle produced even while the bus is arbitrated away from the processor must look exactly like an **8 MHz** 68000 bus cycle. This constraint is necessary to provide the proper sharing of the memory between the processor and the video. In all transfers, DTACK must be provided/sampled as required by the 68000 processor specification. Also, transfers may not last more that 64 clock cycles. The ST will automatically generate a bus error if AS is held low for more than 64 clock cycles.

The diagram below shows a top view of the connector on the motherboard with its associated pin numbers and signal names. This connector (TRW no. 009-00002-8, JAE no. ME03-R64P-D4T2-A1 or equivalent) is the male side. The expansion board uses the female side (TRW no. 009-00005-6, JAE no. ME03-64S-D4R1-A1 or equivalent). See the attached drawings for more specific information on the connector and how it should be mounted.



Top View of Motherboard Connector

The following is a brief description of each signal on the connector. For more detailed information consult a 68000 processor data sheet.

CLK

This signal is an 8.0106 MHz TTL compatible, 50% duty cycle, square wave.

$\overline{\text{RESET}}$, $\overline{\text{HALT}}$

In combination these two signals can be used to indicate a system reset. RESET can be used by itself to indicate a system or software reset (RESET instruction executed). These are both bidirectional (open collector) signal terminated on the motherboard with a 1K and a 4.7K pullup respectively. They may be driven according to standard 68000 processor timing to acheive the functions of the 68000's RESET and HALT lines.

A system reset will occur at powerup and any time the reset switch pressed. It causes both lines to go low for at least 1 mS. A software reset will cause only the RESET line to go low for approximately 15 uS.

A1 - A23

These lines provide the 23-bit address directly from the 68000 processor. They are terminated on the motherboard with 4.7K pullups.

D0 - D15

This is the 16-bit bidirectional data bus. It is terminated on the motherboard with 10k pullups.

FC0, FC1, FC2

These lines indicate the processor status for the current bus cycle. They are directly driven by the 68000 processor. They are terminated on the motherboard with 10K pullups.

$\overline{\text{AS}}$

When this signal is low it indicates that a valid address is on the address lines. It is terminated on the motherboard with a 4.7K pullup.

R/$\overline{\text{W}}$

When high indicates the processor is doing a read cycle. When low indicates the processor is doing a write cycle. Terminated on the motherboard with a 4.7K pullup.

$\overline{\text{UDS}}$, $\overline{\text{LDS}}$

In the case of a write, when UDS is low valid data is available on the upper byte of the data bus. Similarly, when LDS is low valid data is available on the lower byte of the data bus. During a read, the upper byte of the data bus should be driven when UDS is low, and/or the lower byte should be driven when LDS is low. The lines are terminated

on the mother board with 4.7K pullups.

$\overline{\text{DTACK}}$

This bidirectional (open collector) line is used to indicate a completed data transfer. An expansion device which is being driven by the processor must generate this signal to acknowledge the transfer. An expansion device which does DMA must watch this signal to insure the transfer is complete. This line is terminated on the motherboard with a 1K pullup.

$\overline{\text{BERR}}$

This open collector line is used to tell the processor or DMA device that no peripheral device has responded to the current bus cycle. The ST will automatically generate this signal if a bus cycle does not complete within 64 clock cycles. This line is terminated on the motherboard with a 4.7K pullup.

E

This is an enable clock to be used with 6800 type peripherals. It will be low for six clocks and high for four clocks.

$\overline{\text{VPA}}$

This open collector line is used to indicate that a 6800 type cycle should be executed. It is terminated on the motherboard with a 4.7K pullup.

$\overline{\text{VMA}}$

This signal is used to syncronize 6800 type bus cycles with the enable clock.

$\overline{\text{BR}}$

This open collector line is used to request that the processor relinquish the bus to the peripheral. It is terminated on the motherboard with a 4.7K pullup. If it is used on the expansion board it should also be terminated there with another 4.7K pullup.

$\overline{\text{BG}}$

This signal indicates that the bus will be released at the end of the current bus cycle. This signal is daisy chained through the other DMA devices on the ST motherboard. It does not come directly from the processor.

$\overline{\text{BGACK}}$

This open collector signal is used by a DMA device to claim bus mastership. It is terminated on the motherboard with a 4.7K pullup. If it is used on the expansion board it should also be terminated there with another 4.7K pullup.

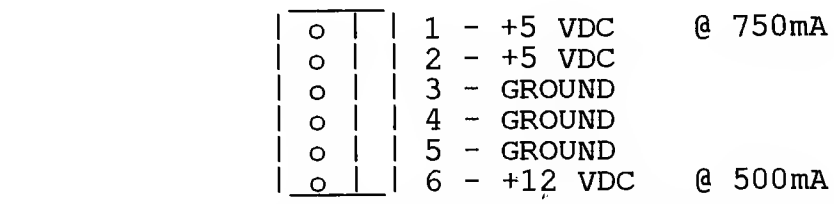
$\overline{\text{NMI}}$, $\overline{\text{INT 5}}$, $\overline{\text{INT 3}}$

These signals are used to asyncronously generate a level 7, level 5, or level 3 interrupt. These are the only levels which can be externally generated. If they all occur

simultaneously, the highest priority (level 7) will be acknowledged first. The expansion card is responsible for responding to any interrupt acknowledges for interrupts which it generates. These acknowledges can be either vectored or auto-vectored. All three lines are terminated on the motherboard with 1K pullups.

Power

Power is supplied to the expansion card through a pigtail cable which plugs onto a six pin connector on the motherboard. The connector on the motherboard is Amp no. 171825-6. The mating connector on the pigtail from the expansion board is Amp no. 171822-6. The pin out and drive capabilities are as follows:



The pigtail should be capable of extending 12cm from the 0,0 location shown on figures 1 and 2.

Software Considerations

The mediation of available addresses should not be necessary since only one expansion card may be plugged in at a time. Atari has set aside the addresses C00000 through CFFFFF, FF0000 through FF7FFF and FFFE00 through FFFFFD for use by outside developers. (Spurious acesses to FFFFFE/FFFFFF may be generated) Atari reserves the right to freely use any other address.

A word of caution to add-on memory vendors, you can't add RAM which will work as video memory and/or will allow DMA. Also, if memory is extended on the expansion card, the operating system will not clear it or allow it to be allocated.